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Engineering Note

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Project: CFT Axial
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Subject: Possible methods for variable gain in the SIFT input

This note disusses SPICE efforts to determine if a 'variable gain' switch is possible for the SIFT input. Four different configurations are analyzed:

- Series JFET using the gate-source capacitance as the 'bleed' capacitance that removes charge from the SIFT;
- Parallel JFET using the JFET as a switch to add a parallel capacitance to allow more charge into the SIFT;
- Shunting JFET, using the JFET as a switch to change the shunt capacitance;
- Shunting diode, using a varactor diode as a variable shunt capacitor.

Stimulus

The same stimulus is used in all setups. Current source I3 is an exponential pulse as shown in Figure 2. Figure 1 shows the exact parameters of the pulse.

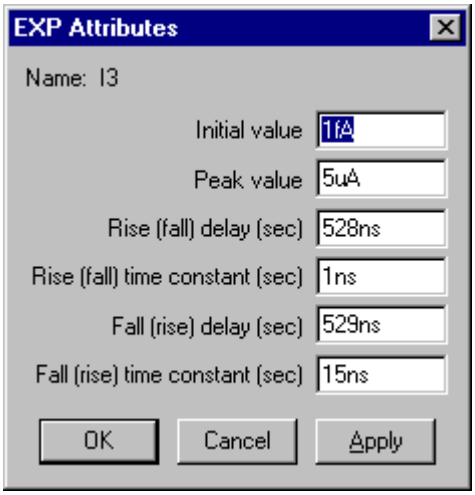

Figure 1

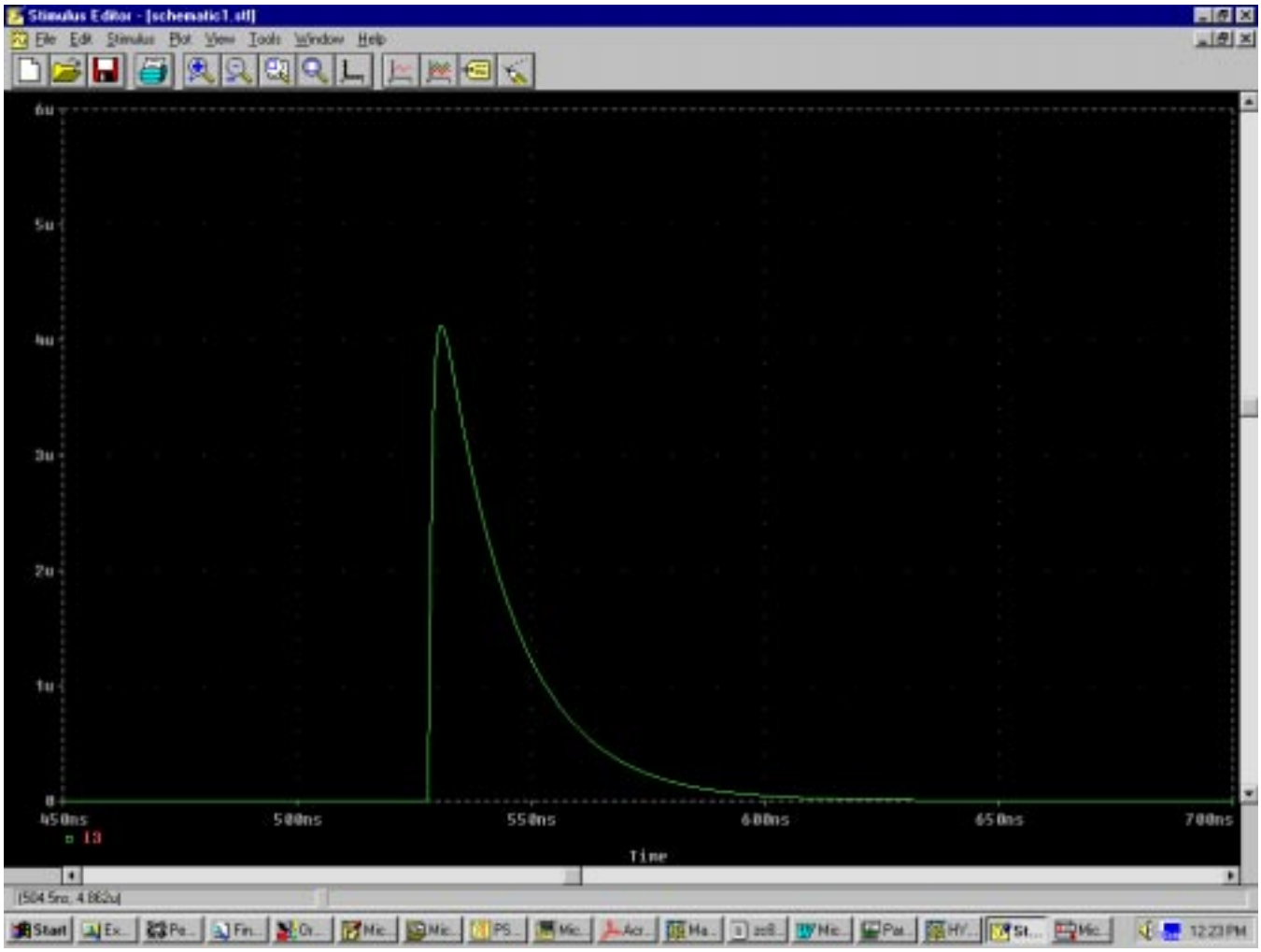

Figure 2

This stimulus is used in various circuits to emulate the VLPC charge.

Series JFET, using gate-source capacitance as bleed

This technique tries to use the gate-source capacitance of the JFET, bled down through the power supply V8, as a variable bleed capacitance. Figure 3 shows the schematic. The gate-source capacitance should split the charge, varying the amount going through C16 to the SIFT. R28 estimates the output impedance of the amplifier and/or DAC which would be used to derive the control voltage. As shown in Figure 4, a varying current is applied to the SIFT (modeled by R19), but noise is introduced which we'd rather avoid.

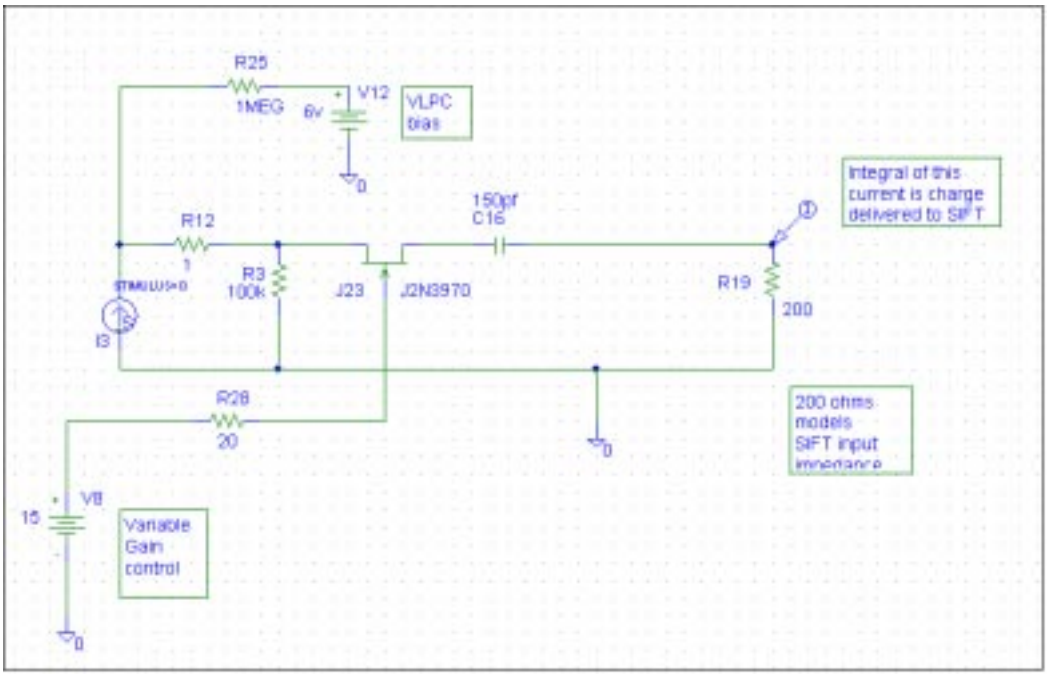

Figure 3

Integrated Charge

Current into SIFT

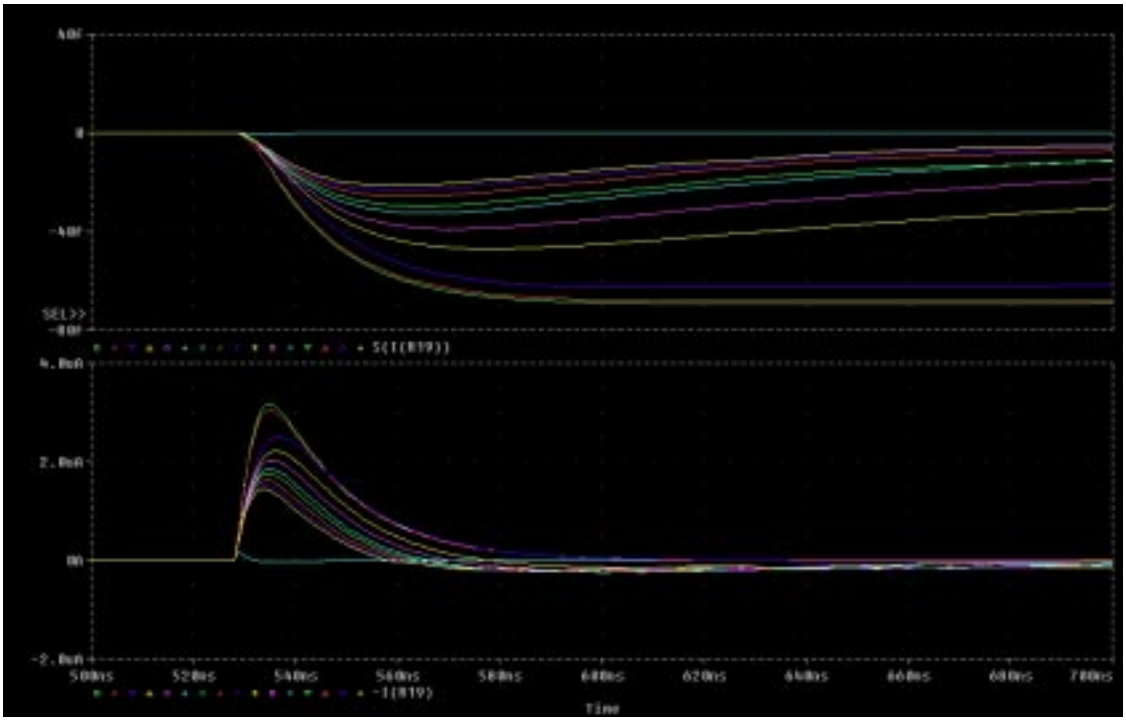

Figure 4

The upper trace shows the integrated charge seen by the SIFT, the lower trace is the current into the SIFT. Not a very good result.

Parallel JFET

A second idea is to try and use the JFET to change the feed-forward portion of the circuit, while having a fixed shunt capacitance. This is shown in Figure 5:

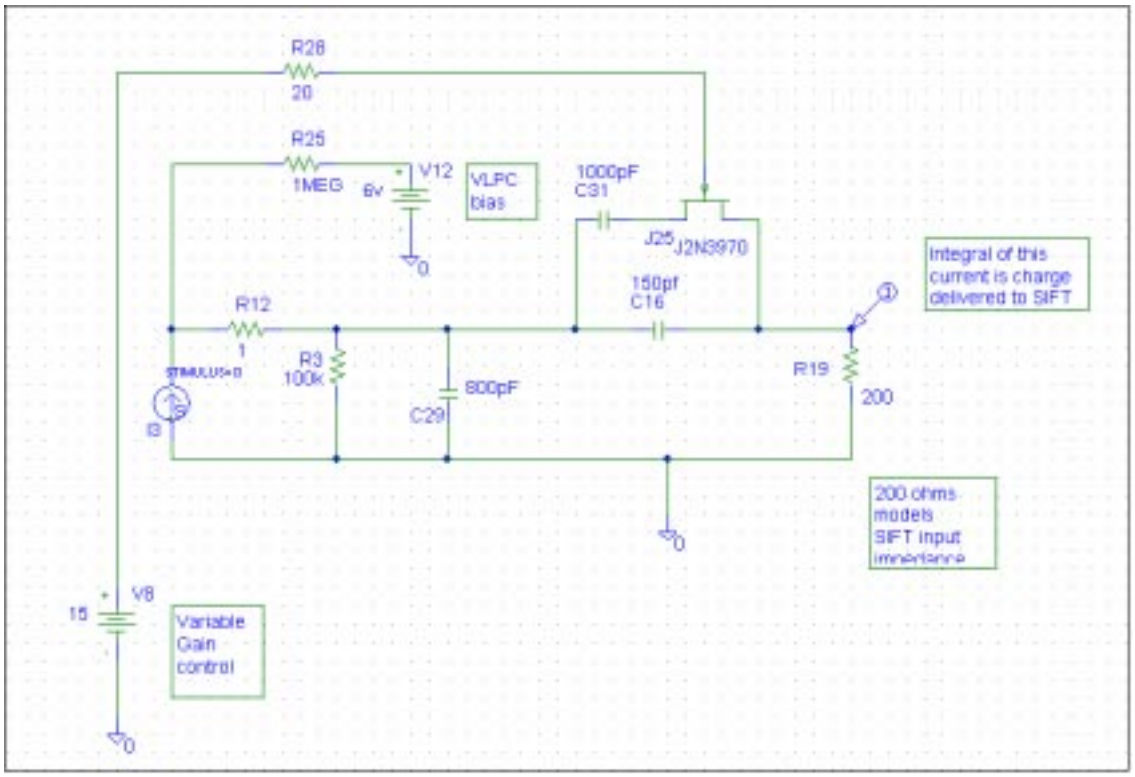

Figure 5

This circuit fails because the time constant of the delivered charge changes with the FET control voltage, as shown in Figure 6.

Integrated charge

Current into SIFT

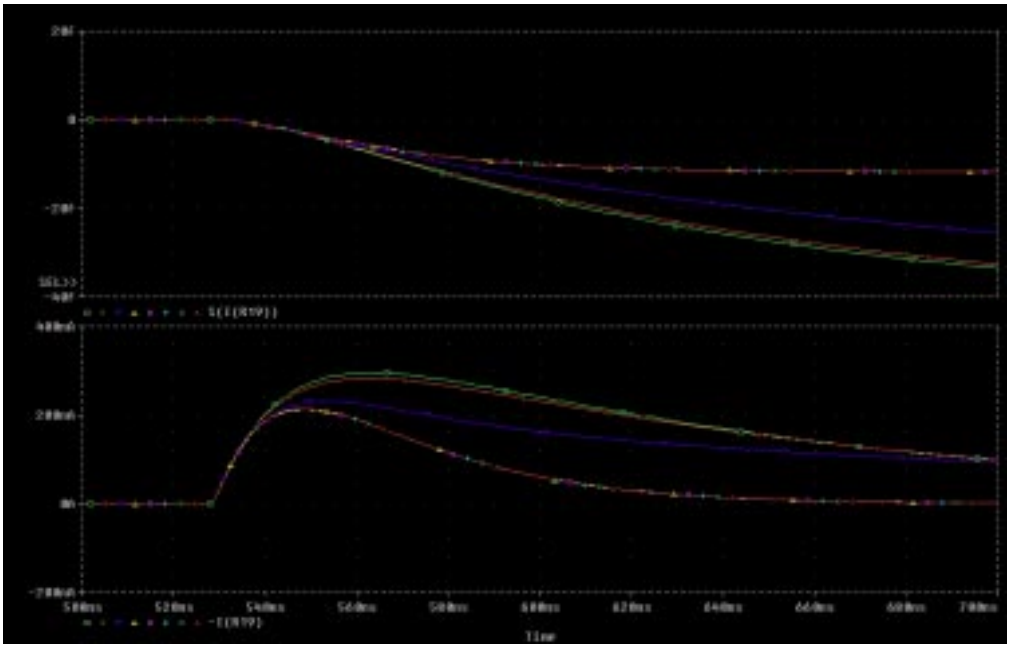

Figure 6

Shunting JFET, JFET as switch

Option 3 is to use the analog switch to optionally add capacitance in the shunt leg, as shown in Figure 7.

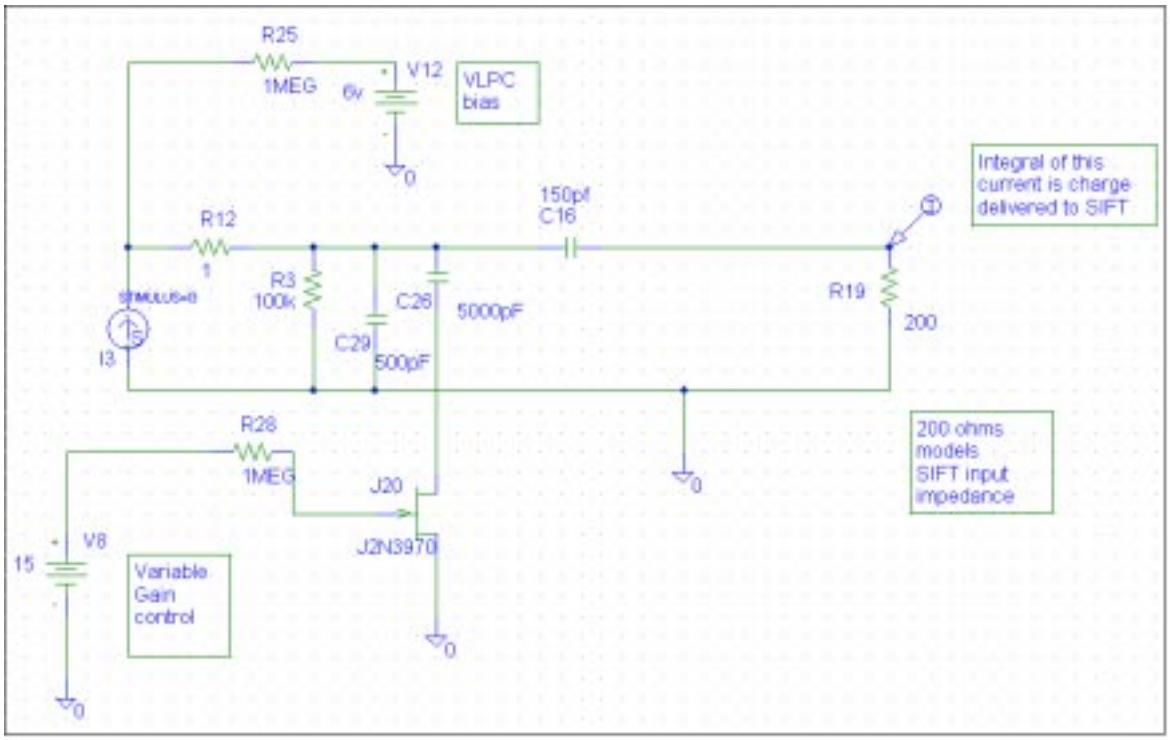

Figure 7

The results again are unsatisfying because of the pulse width degredation, shown in Figure 8.

Integrated charge

Current into SIFT

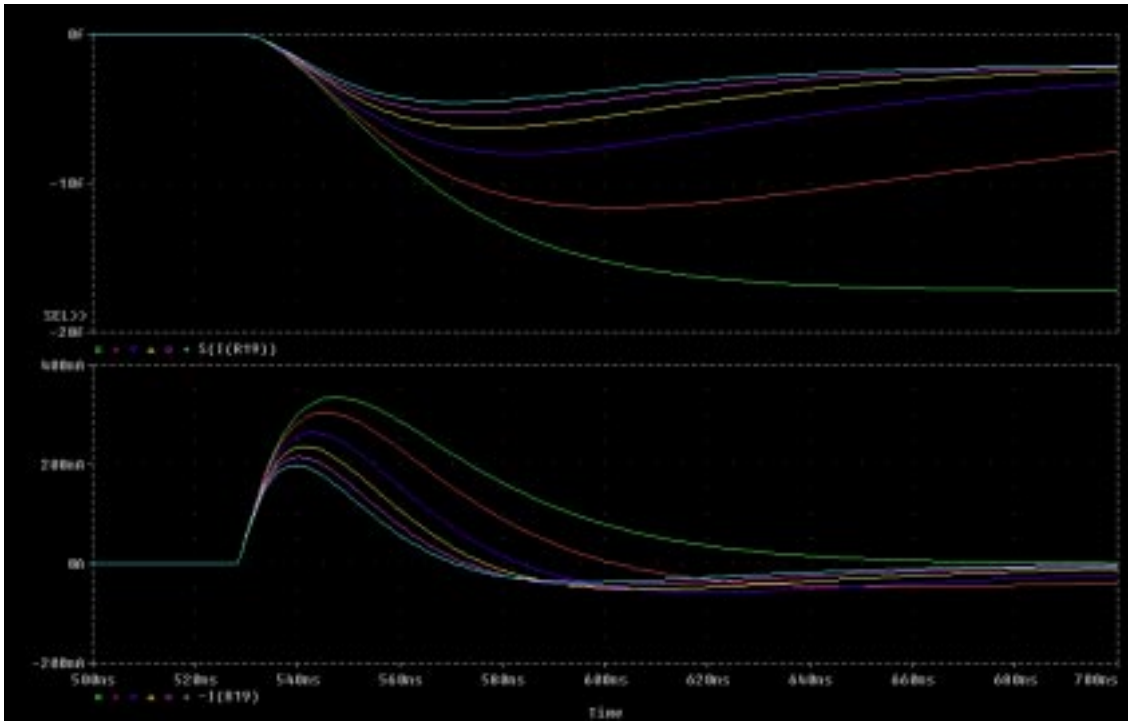

Figure 8

Varactor (voltage-variable capacitance) diode shunt

The last option is to use a voltage-variable diode to create a variable shunt capacitance. A Zetex ZC826A diode was chosen based upon the wide variability as opposed to other devices. Figure 9 shows the schematic.

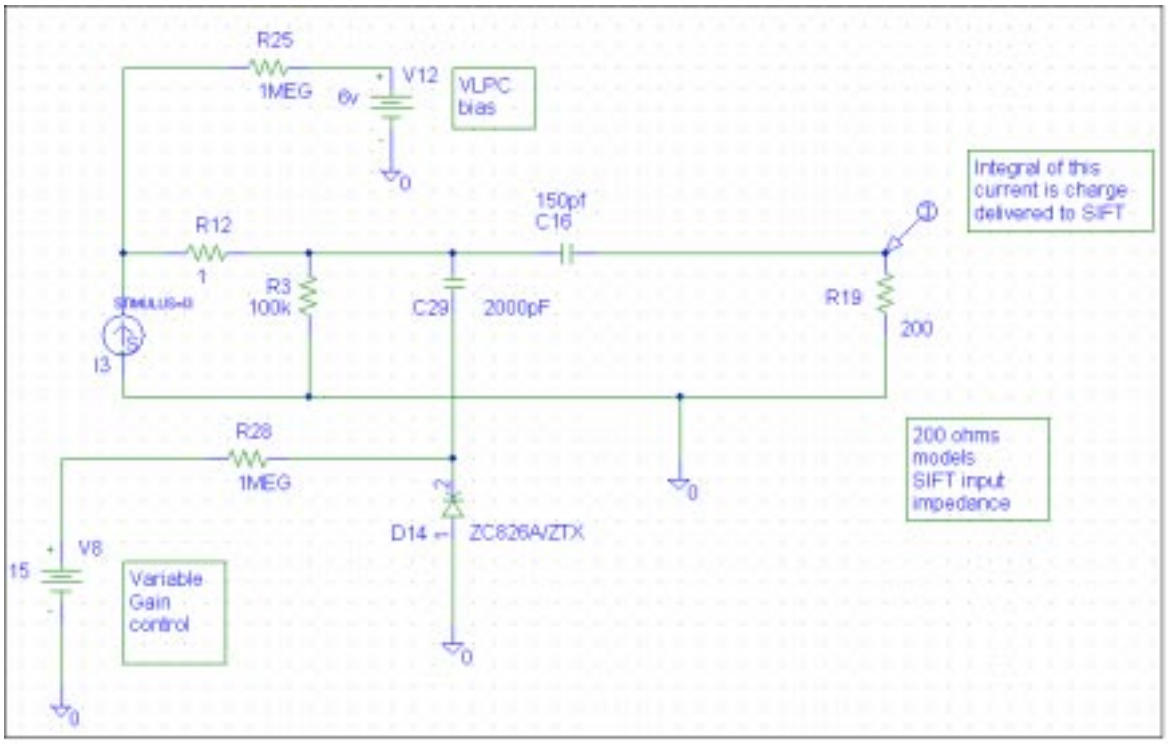

Figure 9

The tuning diode appears to be much more pleasant than the transistor options, as shown by the plots in Figure 10.

Integrated charge

Current into SIFT

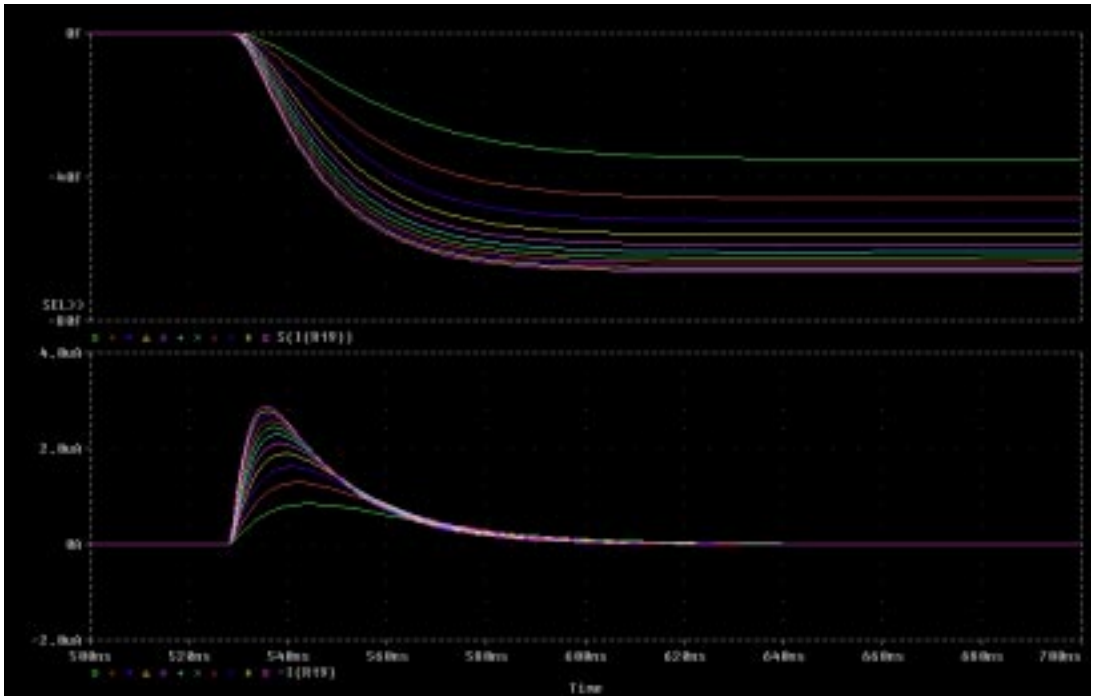

Figure 10

To double-check the validity of the plots, the latest spice model for the device was downloaded from the Zetex web site and the simulation re-run.

Conclusions

1. Use of a varactor diode appears to allow variable gain into the SIFT without introducing excess noise.
2. Gain variation over a 2:1 or, possibly, a 3:1 range appears possible, but 10:1 isn't in the cards.
3. Given the wide range of settings already available in the SIFT, an additional factor of 2 isn't worth the risk of introducing noise problems by additional components.